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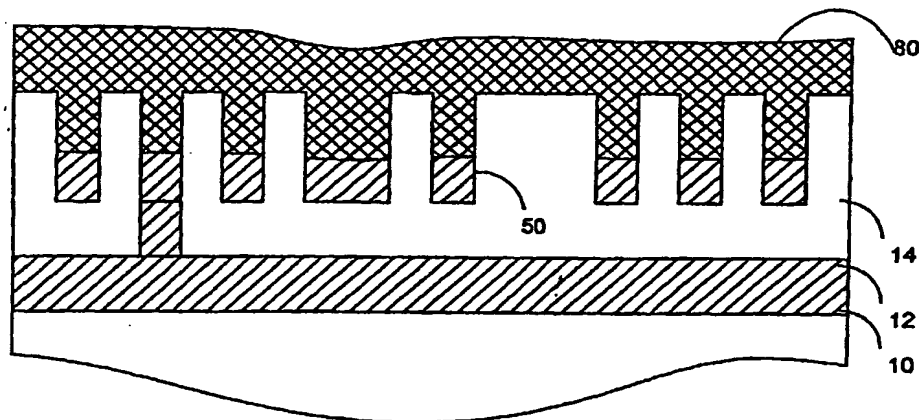
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ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF PRODUCING COPPER FEATURES ON SEMICONDUCTOR WAFERS



(57) Abstract: Copper or a copper containing compound is deposited in holes or depressions in a substrate, and the copper material is oxidized to fill voids and defects in the copper material, and then reduced to produce a uniform filling of the depression by elemental copper.

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Method of producing copper features on semiconductor wafers

FIELD OF THE INVENTION

The field of the invention is the field of producing features formed of copper in grooves and holes in a surface of a substrate. The invention is of particular use in the field of semiconductor processing and the providing of copper lines and vias on a semiconductor substrate.

BACKGROUND OF THE INVENTION

The main stream of semiconductor processing has heretofore been concerned with silicon processing where devices of p and n type doped silicon are interconnected in large numbers by conducting wires. These wires have typically been made from aluminum with slight admixtures of silicon or other material to inhibit electromigration of the metal. Unfortunately, the conductivity of aluminum is too small to provide the low resistance needed for increasingly narrow lines. Recently, copper has been used to great advantage, since research has led the way to providing barrier layers which keep copper from contaminating the silicon. However, the well known problems of filling narrow, deep trenches and holes with a metal still have problems in providing material lacking in voids and defects which raise the resistance and lower the stability of the conducting lines.

Fig. 1 shows a sketch of a typical cross sectional view of a construction of a substrate 10, which may here be a semiconductor such as silicon, gallium arsenide, or gallium nitride or other electronic material, or may be a finished layer of insulator or metal or insulator with buried metal wires or vias. A layer 12 is shown as an example laid on top of layer 10, where layer 12 may be a wire stretching across the substrate. An insulator 14 such as silicon dioxide or any other insulator known in the art of semiconductor processing is shown formed on layer 12, and insulator 14 has been etched to form trenches 16 at intervals in the top of layer 14. A plug 18 is shown schematically to show an electrically conducting connection between layer 12 and following layers of metal to be built up in further steps.

Fig. 2 shows schematically the results of filling the trenches 16 of fig. 1 with metal 20.

Layers of different materials such as tantalum and titanium nitride which are used as diffusion barriers to prevent material 20 from diffusing through material 14 and adversely affecting semiconductor material placed below material 14 are not shown in fig. 2. Voids 22 which often form due to the failure of metal 20 to completely fill the trenches 16 are shown schematically. Prior art techniques may rapidly melt the metal 20 using pulsed lasers, which have the effect of filling in the trenches 16 and causing the voids 22 to disappear. However, the cost and complexity of such systems and the difficulty of adjusting the energy fluence from the lasers make such schemes impractical in production.

RELATED PATENTS AND APPLICATIONS

Reactors based on the RTP principle often have the entire cross section of one end of the reactor chamber open during the wafer handling process. This construction has been established because the various wafer holders, guard rings, and gas distribution plates, which have significantly greater dimensions and may be thicker than the wafers, must also be introduced into the chamber and must be easily and quickly changed when the process is changed or when different wafer sizes, for example, are used. The reaction chamber dimensions are designed with these ancillary pieces in mind. US Patent 5,580,830 teaches the importance of the gas flow and the use of an aperture in the door to regulate gas flow and control impurities in the process chamber.

The importance of measuring the temperature of the wafer using a pyrometer of very broad spectral response is taught in U. S. Patent 5,628, 564.

The wafer to be heated in a conventional RTP system typically rests on a plurality of quartz pins which hold the wafer accurately parallel to the reflector walls of the system. Prior art systems have rested the wafer on an instrumented susceptor, typically a uniform silicon wafer. Copending patent application 08/537,409 teaches the importance of susceptor plates separated from the wafer.

Rapid thermal processing of III-IV semiconductors has not been as successful as RTP of silicon. One reason for this is that the surface has a relatively high vapor pressure of, for example, arsenic (As) in the case of gallium arsenide (GaAs). The surface region becomes

depleted of As, and the material quality suffers. Copending patent application 08/631,265 supplies a method and apparatus for overcoming this problem.

A method of raising the emissivity of a lightly doped, relatively low temperature wafer by locally heating the wafer with a pulse of light is disclosed in copending application 08/632,364.

A method, apparatus, and system for RTP an object is disclosed in copending application 08/953,590, filed Oct. 17, 1997, by Lerch et al.

A method of RTP of a substrate where a small amount of a reactive gas is used to control the etching of oxides or semiconductor is disclosed in copending application 08/886,215, by Nenyai et al, filed July 1, 1997.

A method of RTP of a substrate where evaporation of the silicon is controlled is disclosed in copending application 09/015,441, by Marcus et al. filed Jan. 29, 1998.

A method of producing silicon oxynitride films is disclosed in application 09/212,495, by Kwong et al, filed on 12/15/98.

Methods of rotating the wafer in an RTP system are disclosed in applications 08/960,150 and 08/977,019 by Bliersch et al. and Aschner et al. filed on 10/29/97 and 11/24/97 respectively, and in application number 09/209,735 by Aschner et al. filed on 12/11/98.

A cooled showerhead for RTP applications is disclosed in application number 09/245,139 by Walk et al filed 02/04/99.

The above identified applications are assigned to the assignee of the present invention and are hereby incorporated herein by reference.

OBJECTS OF THE INVENTION

It is an object of the invention to produce metal conducting lines and vias and other features in depressions, holes, and trenches in a substrate such as a semiconductor substrate or a semiconductor substrate covered with one or more layers of insulating or conducting films.

It is an object of the invention to produce an apparatus and a system for producing metal conducting lines and vias and other features in depressions, holes, and trenches in a substrate such as a semiconductor substrate or a semiconductor substrate covered with one or more layers of insulating or conducting films.

SUMMARY OF THE INVENTION

A conducting metal or metal containing compound is deposited in holes or trenches in a substrate, and the metal or metal containing compound is oxidized and then reduced. The metal is most preferably copper.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a sketch of a prior art trenched substrate.

Fig. 2 shows the prior art results of filling the trenches of fig. 1 with metal.

Fig. 3 shows the metal of fig. 2 oxidized to form metal oxide material.

Fig. 4 shows the metal oxide material of fig. 3 reduced to form metal.

Fig. 5 shows the results of a first step of an alternative preferred embodiment of the invention.

Fig. 6 shows the results of the second step after fig. 5.

Fig. 7 shows the results of the third step after fig. 6.

Fig. 8 shows the results of the fourth step after fig. 7.

Fig. 9 shows the results of the fifth step after fig. 8.

Fig. 10 shows a system for carrying out the method of the invention.

Fig. 11 shows an SEM micrograph of a control sample of a specimen.

Fig. 12 shows the results of the oxidation of the material of fig. 11.

Fig. 13 show results of reducing a dry oxide film.

Fig. 14 show results of reducing a wet oxide film.

DETAILED DESCRIPTION OF THE INVENTION

The most preferred embodiment of this invention is to coat a copper thin film on a semiconductor wafer for the purpose of interconnecting integrated circuitry. Copper is expected to be integrated into advanced metallization schemes as a low resistance and highly reliable interconnect material. Cu is a promising material for interconnects in ULSI devices because of

low bulk resistivity and high resistance to electromigration compared with Al and its alloys. Recently, much research on Cu metallization has been conducted using various deposition technique such as metal-organic chemical vapor deposition (MOCVD), sputtering, electroless deposition, electrochemical deposition (ECD) etc. CVD holds promise for the future, especially as device features shrink, but physical vapor deposition (PVD) and ECD are presently more cost effective. PVD is limited in achieving complete fill by the aspect ratio of the feature but can be used successfully at lower aspect ratios and for deposition of thin barrier and copper seed layer for ECD copper. ECD is effective in achieving complete fill at aggressive aspect ratios and feature sizes of less than 0.25 micron. However, small voids and seams in the center of small trench and via is still the challenge for this technology. Ion assisted deposition of copper has recently been introduced to assist in placing copper deep into trenches to seed the bottom of the trench with copper for following electroless deposition. The combination of directed ion flow (usually perpendicular to the average surface of the substrate) and random walk flow of the uncharged copper atoms supply large quantities of copper to the trench.

Fig. 3 shows a step of the most preferred method of the invention, where the prior art deposited copper deposition 20 shown in fig. 2 is oxidized to form copper oxide material 30. Since the density of copper oxide is 6.0 grams/cm³ and 6.3 grams/cm³ for Cu₂O and CuO respectively, compared with 8.96 grams/cm³ for elemental copper, the voids 22 and defects in the copper are "squeezed out", and the trenches 16 and holes in the surface are filled by the expansion of the material. It is only necessary to oxidize the copper material 20 to a depth below the defects or voids 22, and not to the bottom of the trenches 16, in order to achieve good results in the subsequent copper reduction step.

When the copper oxide material 30 is reduced in a reduction step, elemental copper 40 remains as shown in fig. 4, and fills the trenches 16 without voids or gross defects. The copper oxide reduction is exothermic, producing 76.97 kJ/mole and 89.43 kJ/mole energy for Cu₂O and CuO respectively. The heat capacity of copper varies from 5.84 to 7.6 cal/mole °K as the temperature is raised from room temperature to the melting point of copper. A free standing film of copper oxide will thus heat up when reduced to copper in the absence of heat transfer. Such heating would anneal the copper and produce superior material for electronic operations. If heat

transfer by radiation, convection, and conduction to the surrounding is taken into account, the reduction of the copper oxide material 30 to elemental copper 40 must be done sufficiently fast that the heat production rate from the reduction is greater than the heat loss rate from the resulting film.

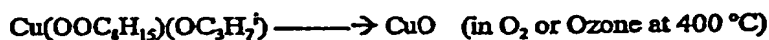
Fig. 5 shows an alternative preferred embodiment of the invention, where the trenches 16 are partially filled with copper or a copper containing material 50. The material 50 is converted to copper oxide 60 of fig. 6 in an oxidation step similar to that shown in fig 3. The copper oxide material 60 partially filling the trench is reduced to elemental copper 70 as shown in fig. 7, and new copper containing material 80 is deposited on top of the copper material 50. Continuing cycles of deposition, oxidation, and reduction will finally fill in the trenches 16 and produce trenches filled with void free copper 90 as shown in fig. 9. In this embodiment, it is not necessary to completely oxidize the previous copper layer. The copper containing material may be copper deposited according to any of the prior art processes, or it may be organic material containing copper, or it may be copper oxide or copper powder.

The Cu oxidation may be carried out in wet or dry oxygen containing gas. The reactions are:



Organic Cu compounds can be dissolved in certain solvents. These low viscosity liquid solutions could be very useful for the deep submicron technology. For examples, copper ethylhexano-isopropoxide ($\text{Cu}(\text{OOC}_6\text{H}_{13})(\text{OC}_3\text{H}_7)_2$) can be dissolved in isopropanol; copper 2-methoxyethoxide ($\text{Cu}(\text{OCH}_2\text{CH}_2\text{OCH}_3)_2$) can be dissolved in 2-methoxyethanol, and copper(II) 2-ethylhexanoate ($\text{Cu}(\text{OOC}_6\text{H}_{13})_2$) can be dissolved in toluene. The low viscosity material may be sprayed, dipped, or spun on to the substrate surface and will fill the trenches and holes. The oxidation and reduction reactions for these material are:

Cu Oxidation





Cu Oxide Reduction



Fig. 10 shows a system for carrying out the method of the invention. A copper coating apparatus 100 is used to coat a substrate with a layer of copper containing substance. Such an apparatus is any one or a combination of systems such as metal-organic chemical vapor deposition (MOCVD), sputtering, electroless deposition, electrochemical deposition (ECD), ion assisted copper deposition for depositing elemental copper on the substrate. Apparatus for applying a copper containing substance in liquid form include but are not limited to jet spraying, electrophoresis, spraying, electrospraying, dipping, spin coating, static electric charged droplet coating, etc. Apparatus for dry coating include but are not limited to apparatus for dry powder coating, electrostatic dry powder application apparatus, etc. The substrates are transferred between apparatus 100 and an oxidation/reduction apparatus 104 by a wafer handling system 102. Wafers are loaded and unloaded to and from the wafer handling system 102 as denoted by the arrow 107. Typically, a cassette containing 25 wafers is loaded into system 102, and a mechanical arm removes the wafers one at a time and introduces them into system 100. When the wafer has been coated with the copper containing material, it is removed by system 102 as shown by arrow 105 and transferred as shown by arrow 106 to the system 104 for an oxidation step followed by a reduction step. After the reduction step, the wafer is removed from system 104 by system 102 as shown by arrow 106. The wafer may be reinserted back into system 100 for further coating of the copper containing material, or may be loaded back into the cassette for eventual removal to the next processing step. The system shown in fig. 10 is necessary for repeat operations of the deposition, oxidation, and reduction embodiment of the invention. The oxidation and reduction operations require utmost cleanliness, and can be carried out only with difficulty in an apparatus which is used as a deposition apparatus.

The preferred apparatus for oxidation and reduction is a rapid thermal processing (RTP) apparatus. While tube furnaces may be used to advantage for the reduction and oxidation steps,

wafers may be handled one at a time by an RTP system, which is very important for the practice of the invention if multiple coating steps are necessary. In addition, RTP systems may raise the temperature of the substrate at rates of up to 1000°C per second, which leads to very rapid reduction of the copper oxide film and consequent rapid heating of the resultant copper film. The most preferred embodiment of the invention raises the temperature of the copper oxide film by at least 50 °C per second. Less preferred embodiments raise the temperature of the copper oxide film by 20 °C per second and by 5 °C per second.

Fig. 11 shows an SEM micrograph of a specimen broken from a substrate (an 8 inch wafer) covered with a silicon dioxide film 110 which has been etched to give trenches 112 approximately 0.3 microns wide and 0.5 microns deep. Copper 114 has been deposited on the silicon dioxide film. A void 116 is shown in the left hand side of the trench. The specimen shown in fig. 11 was cut up to run a series of experiments.

Fig. 12 shows the results of the oxidation of the material of fig. 11. The oxidation was carried out in dry oxygen at 330 °C for 60 seconds. Ellipsometer measurements of the film on a flat part of the wafer indicate that the entire copper film was converted to oxide, but the SEM picture of fig. 12 indicate that the oxide 120 material may not reach the bottom of the trench, and that the material 122 in the bottom of the trench may be copper. Note that there is no sign of the void 116 remaining in the copper oxide material 120, and that the material 120 is much "flatter" on top than the deposited copper metal.

Fig. 13 and fig. 14 show results of reducing the film of fig. 12 in a step where the reducing atmosphere was a forming gas atmosphere having only 10 % hydrogen gas. The temperature of 400 °C and time of 180 seconds were chosen to ensure that the copper oxide was completely reduced. The time for the reduction step could be significantly changed using a higher percentage of hydrogen for the reduction and experimentation as is known in the art to find the minimum time needed to reduce the oxide. Safety systems for high hydrogen partial pressure were, however, not available for the experiments reported. The specimen shown in fig. 14 was oxidized in a wet oxide process. No appreciable difference was noted in the results from wet oxidation and dry oxidation.

Obviously, many modifications and variations of the present invention are possible in

light of the above teachings. It is therefore to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

We claim:

1. A method for filling depressions in the surface of a substrate, comprising:

depositing copper oxide in the depressions; and

reducing the copper oxide to elemental copper by heating the copper oxide in a reducing atmosphere.
- 2.. The method of claim 1, where the substrate is a semiconductor substrate having depressions of characteristic width w and depth d , where d is greater than w .
- 3.. The method of claim 2, where d is greater than $3w$.
4. The method of claim 1, where copper oxide is reduced to elemental copper in a time less than 10 seconds.
5. The method of claim 4, where copper oxide is reduced to elemental copper by rapidly switching an ambient gas atmosphere about the substrate from a non-reducing atmosphere to a reducing atmosphere.
6. The method of claim 4, where copper oxide is reduced to elemental copper by rapidly raising the temperature of the substrate.
- 7.. The method of claim 1, where the copper oxide is reduced to elemental copper in the chamber of a rapid thermal processing system.

8. The method of claim 1, where the step of depositing copper oxide comprises the steps of:

depositing copper in the depressions in the surface of the substrate; and
oxidizing the copper.

9. The method of claim 8, where the step of depositing the copper is carried out by metal-organic chemical vapor deposition (MO-CVD).

10. The method of claim 8, where the step of depositing the copper is carried out by sputtering.

11. The method of claim 8, where the step of depositing the copper is carried out by electroless deposition.

12. The method of claim 8, where the step of depositing the copper is carried out by electrochemical deposition (ECD).

13. The method of claim 8, where the step of depositing the copper is carried out by physical vapor deposition (PVD).

14. The method of claim 8, where the step of depositing the copper is carried out by chemical vapor deposition (CVD).

15. The method of claim 8, where the step of depositing the copper is carried out by ion assisted vapor deposition.

16. The method of claim 1, where the depressions in the surface of the substrate have been previously partially filled with copper.

17. The method of claim 16, where the steps of depositing and of reduction are repeated a plurality of times.
18. The method of claim 1, where copper oxide is deposited in the depressions by deposition of a copper containing compound from a liquid organic copper compound solution, followed by an oxidation step.
19. The method of claim 18, where liquid organic copper compound solution is a solution of copper ethylhexano-isopropoxide ($\text{Cu}(\text{OOC}_2\text{H}_{13})(\text{OC}_3\text{H}_7)_2$).
20. The method of claim 18, where liquid organic copper compound solution is a solution of copper 2-methoxyethoxide ($\text{Cu}(\text{OCH}_2\text{CH}_2\text{OCH}_3)_2$), followed by an oxidation step.
21. The method of claim 18, where liquid organic copper compound solution is a solution of copper(II) 2-ethylhexanoate ($\text{Cu}(\text{OOC}_2\text{H}_{13})_2$), followed by an oxidation step.
22. A system for filling depressions in the surface of a substrate, comprising:
- a system for depositing a copper containing material in the depressions;
 - a rapid thermal processing (RTP) system for sequentially oxidizing the copper containing material to copper oxide by heating the substrate in an oxidizing atmosphere, then reducing the copper oxide to elemental copper by heating the copper oxide in a reducing atmosphere; and,
 - a means for transferring the substrate from the system for depositing to the RTP system.
23. The system of claim 22, where the substrate is a semiconductor substrate having depressions of characteristic width w and depth d , where d is greater than w .

- 24.. The system of claim 23, where d is greater than $3w$.
25. The system of claim 22, where copper oxide is reduced to elemental copper in a time less than 10 seconds.
26. The system of claim 25, where copper oxide is reduced to elemental copper by rapidly switching an ambient gas atmosphere about the substrate from a non-reducing atmosphere to a reducing atmosphere.
27. The system of claim 25, where copper oxide is reduced to elemental copper by rapidly raising the temperature of the substrate.
28. The system of claim 22, where the step of depositing is carried out by metal-organic chemical vapor deposition (MO-CVD) of copper.
29. The system of claim 22, where the step of depositing is carried out by sputtering of copper.
30. The system of claim 22, where the step of depositing is carried out by electroless deposition of copper.
31. The system of claim 22, where the step of depositing is carried out by electrochemical deposition (ECD) of copper.
32. The system of claim 22, where the step of depositing is carried out by physical vapor deposition (PVD) of copper.
33. The system of claim 22, where the step of depositing is carried out by chemical vapor deposition (CVD) of copper.

34. The system of claim 22, where the step of depositing is carried out by ion assisted vapor deposition of copper.

35. The system of claim 22, where the steps of depositing, and of reduction are repeated a plurality of times.

36. A system for filling depressions in the surface of a substrate, comprising:

a system for depositing copper oxide in the depressions;

a rapid thermal processing (RTP) system for reducing the copper oxide to elemental copper by heating the copper oxide in a reducing atmosphere; and,

a means for transferring the substrate from the system for depositing copper oxide to the RTP system.

37. A system for filling depressions in the surface of a substrate, comprising:

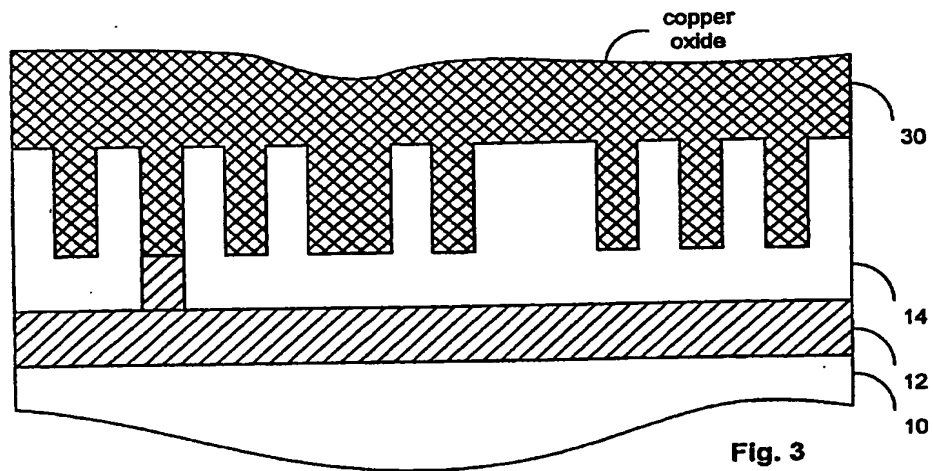
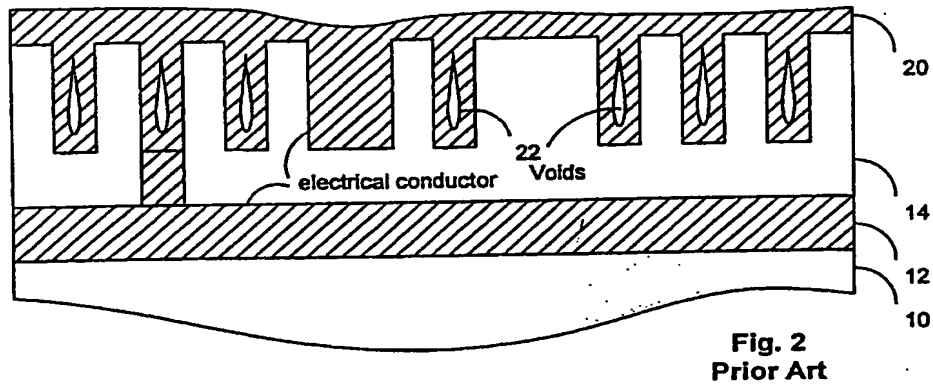
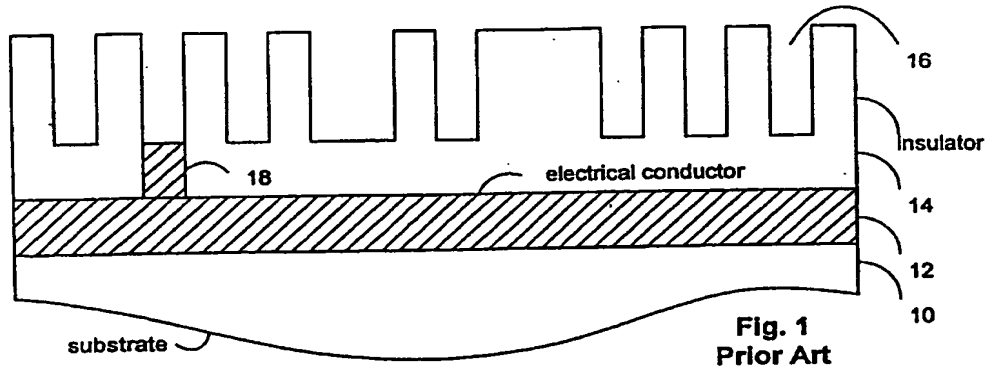
a system for depositing a copper organic compound in the depressions;

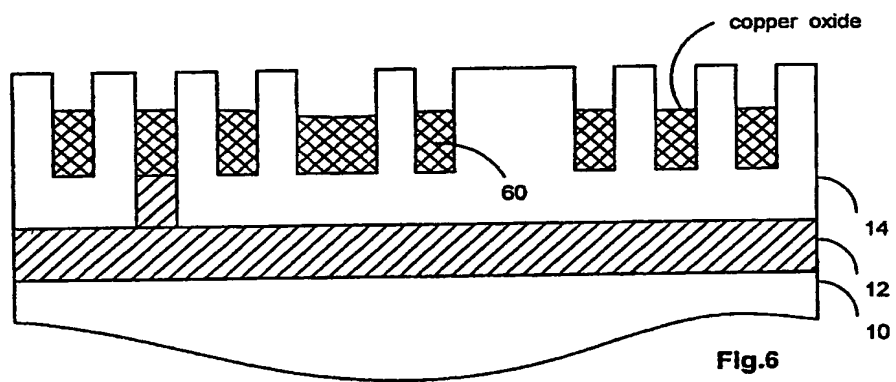
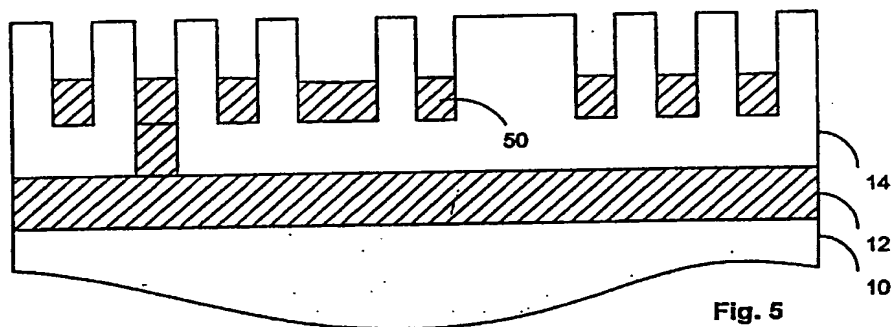
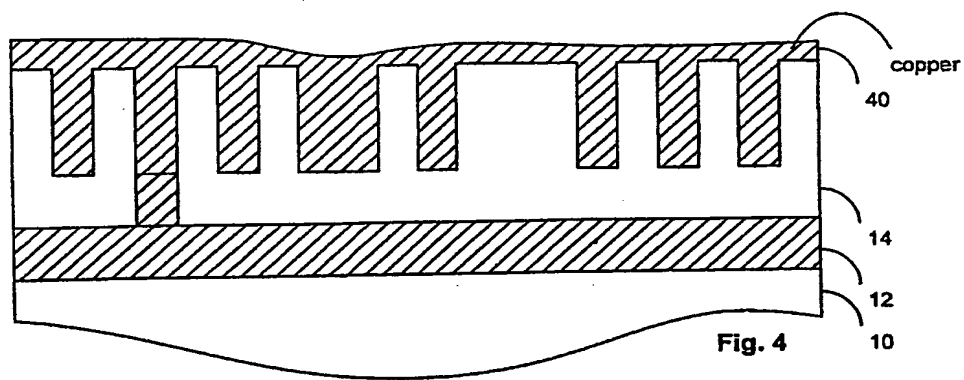
a rapid thermal processing (RTP) system for sequentially oxidizing the copper organic compound to copper oxide by heating the substrate in an oxidizing atmosphere, then reducing the copper oxide to elemental copper by heating the copper oxide in a reducing atmosphere; and,

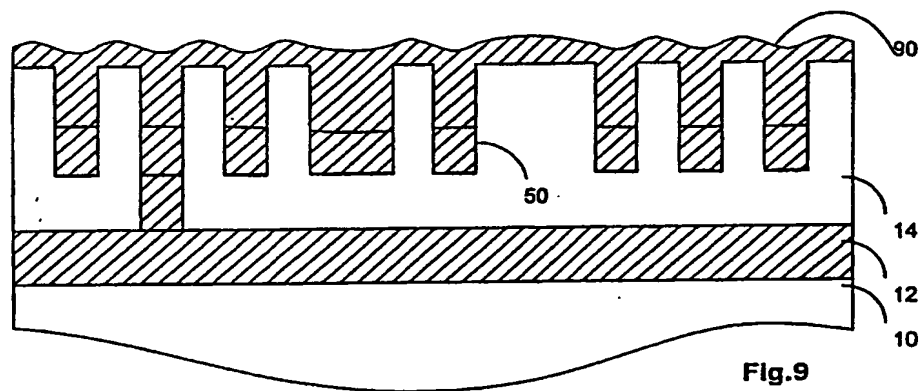
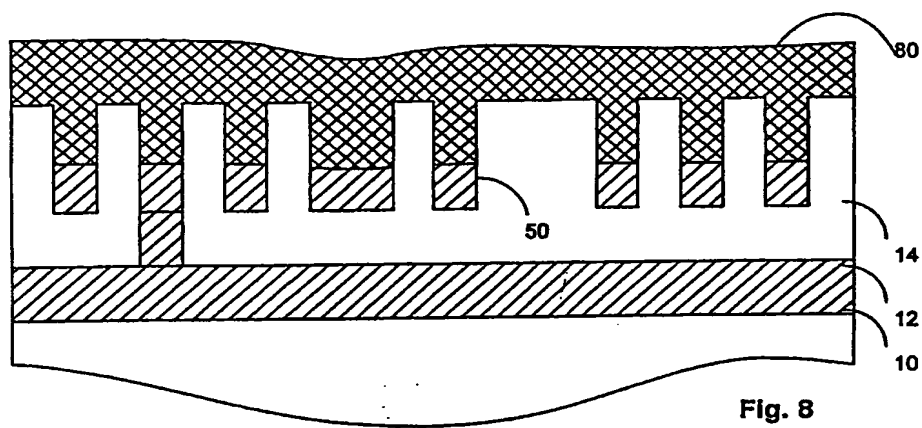
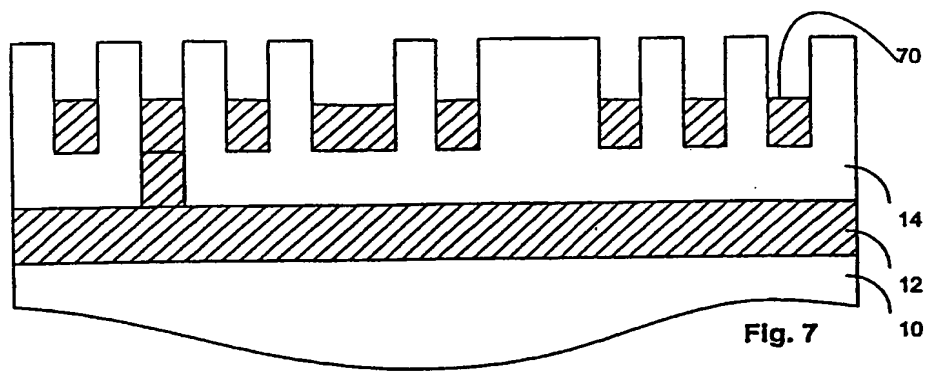
a means for transferring the substrate from the system for depositing to the RTP system.

38. The system of claim 37, where the system for depositing is a spin coater.

39. The system of claim 37, where the system for depositing is a jet spray coater.
40. The system of claim 37, where the system for depositing is a printing coater.
41. The system of claim 37, where the system for is a static-electric spray coater.
42. The system of claim 37, where the system for depositing is a electrophoresis coater.
43. The system of claim 37, where copper organic compound is deposited in the depressions by deposition from a liquid organic copper compound solution.
44. The system of claim 43, where liquid organic copper compound solution is a solution of copper ethylhexano-isopropoxide ($\text{Cu}(\text{OOC}_2\text{H}_{13})(\text{OC}_3\text{H}_7)_2$).
45. The system of claim 43, where liquid organic copper compound solution is a solution of copper 2-methoxyethoxide ($\text{Cu}(\text{OCH}_2\text{CH}_2\text{OCH}_3)_2$).
46. The system of claim 43, where liquid organic copper compound solution is is a solution of copper(II) 2-ethylhexanoate ($\text{Cu}(\text{OOC}_2\text{H}_{13})_2$).







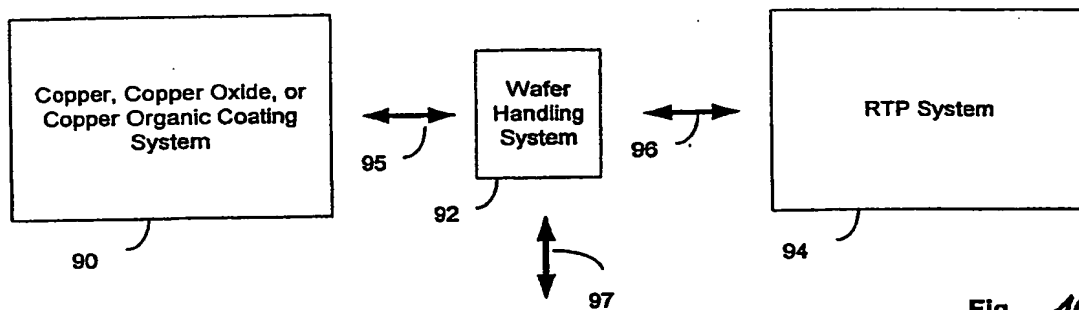




Fig. 11

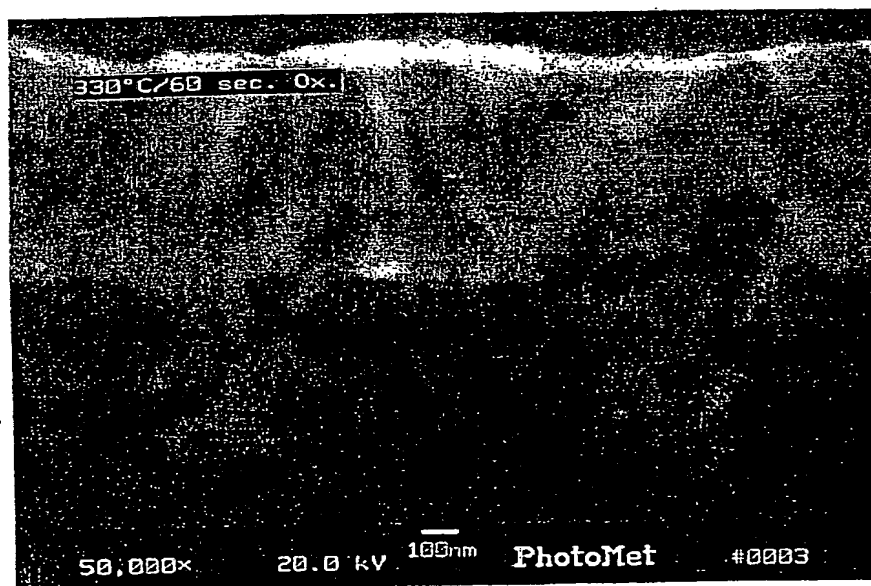


Fig. 12

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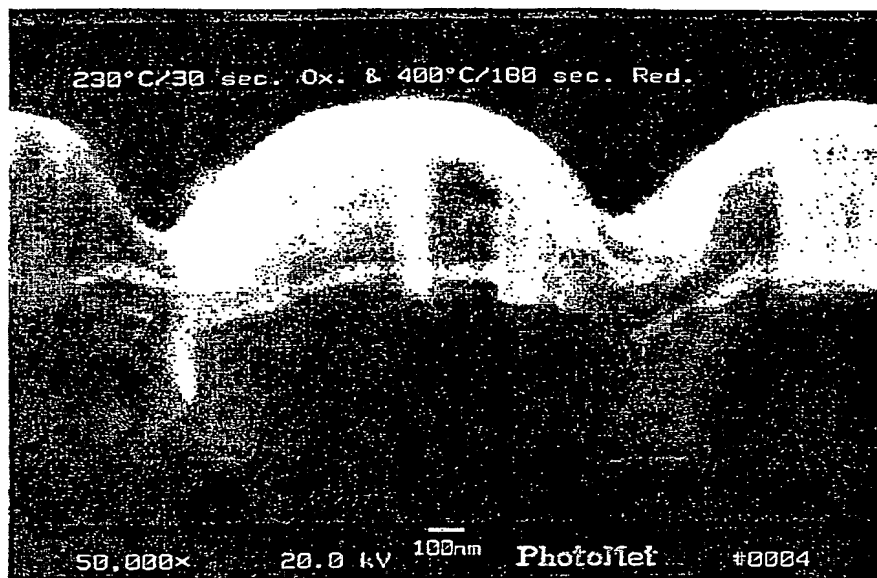


Fig. 13

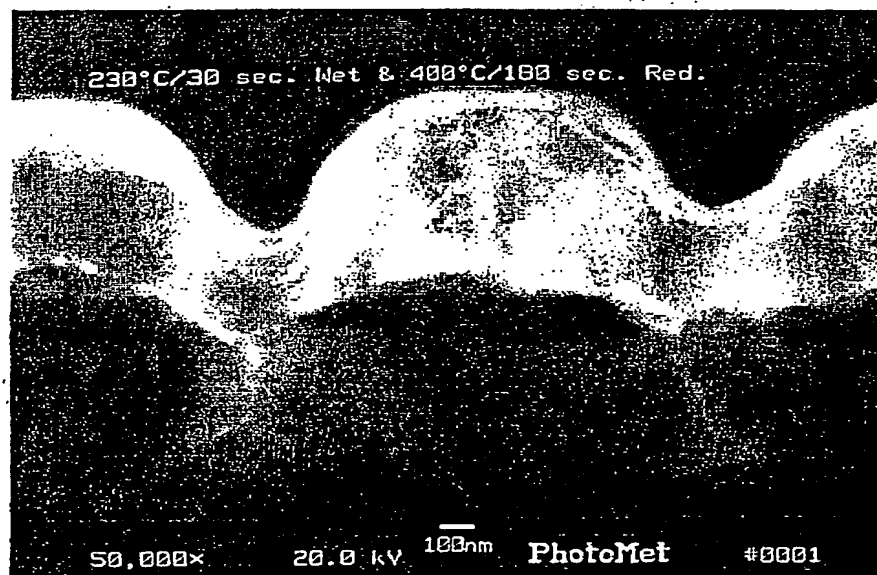


Fig. 14

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 00/01115

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768 H01L21/288

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A P,X A	<p>US 5 424 246 A (MATSUO MIE ET AL) 13 June 1995 (1995-06-13) column 3, line 3 - line 37</p> <p>EP 0 984 488 A (NIPPON ELECTRIC CO) 8 March 2000 (2000-03-08) column 4, line 57 -column 6, line 5</p> <p>US 5 728 626 A (ALLMAN DERRYL D J ET AL) 17 March 1998 (1998-03-17) column 2, line 20 - line 38</p>	<p>1,22,36, 37 2-46</p> <p>1,5-16</p> <p>18-20, 22,36-46</p>

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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14 December 2000

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PCT/IB 00/01115

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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